REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add types 04, 05; Delete type 01.	20 July 83	
B	Remove 2 vendors FSCM 01295, FSCM 50088. Add 1 vendor FSCM 34335 with device types 06, 07, 08.	23 Jan 84	
C	Add block diagram and timing diagram for device types 06, 07, and 08. Remove test requirements for t_{OEZ} and t_{CEZ}.	11 Oct 84	
D	Change value of T_{AZ}.	30 Dec 1985	
E	Add T_{OHZ} for device types 06, 07 and 08. Editorial changes throughout.	4 Apr 1986	

Prepared in accordance with DOD-STD-100

Selected item drawing

REV																		
PAGE																		
REV STATUS OF PAGES	REV	E	E	E	E	E	D	D	C	C	C	E	C	C	E	D	D	E
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Original date of drawing 18 March 1982

PREPARED BY

CHECKED BY

APPROVED BY 18 March 87

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO

TITLE

MICROCIRCUITS, DIGITAL, NMOS, 16K, (2048 X 8) BIT, STATIC RAM

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	81039
REV E		PAGE 1 OF 17

DESC FORM 144 MAR 76 AMSC N/A

5962-E077

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes the requirements for monolithic silicon, digital, N-channel Mos, 16384-bit random access memory microcircuits. This drawing provides for a level of microcircuit quality and reliability assurance for acquisition of microcircuits in accordance with MIL-M-38510.

1.2 Part number. The complete part number shall be as shown in the following example:

81039	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish (3.3)

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Supply voltage variation	Address access time
01	(See 6.9)	5%	90 ns
02		5%	120 ns
03		5%	200 ns
04		5%	200 ns
05		10%	200 ns
06		10%	90 ns
07		10%	120 ns
08		10%	200 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1/2" x 1-1/4") dual-in-line package
Z	C-12 (32 terminal leadless, .450 x .550") chip carrier with castellated instead of chamferred corners and extended pad metallization at terminal number 1.

1.3 Absolute maximum ratings.

V_{CC} supply voltage range	-0.5 V dc to +7.0 V dc 1/
Temperature under bias	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	-1.0 W
Lead temperature (soldering 5 seconds)	300°C
Thermal resistance, junction to case (θ_{JC})	40°C/mW
Junction temperature (T_J)	+150°C
All input or output voltages with respect to ground	6.0 V dc to -0.5 V dc 3/
Output short circuit current:	
Device types 01, 02, 03, 04, 05	20 mA
Device types 06, 07, 08	10 mA

1/ All voltages referenced to V_{SS}.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
3/ Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Input low voltage (V_{IL}):	
Device types 01, 02, 03, and 04	-0.3 V dc to +0.65 V dc 4/
Device type 05, 06, 07, 08	-0.3 V dc to +0.8 V dc
Supply voltage range (V_{CC}):	
Device types 01, 02, 03, and 04	+4.75 V dc to +5.25 V dc 4/
Device type 05, 06, 07, 08	+4.5 V dc to +5.5 V dc
Supply voltage range (V_{SS})	0 V dc 4/
Input high voltage (V_{IH}):	
Device types 01, 02, 03, and 04	+2.4 V dc to V_{CC} +0.5 V dc 4/
Device type 05, 06, 07, 08	+2.0 V dc to V_{CC} +0.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. The country of manufacture requirement of MIL-M-38510 does not apply.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Design documentation. The design documentation shall be in accordance with MIL-M-38510 and, unless otherwise specified in the contract or purchase order, shall be retained by the manufacturer but be available for review by the acquiring activity or contractor upon request.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

4/ All voltages referenced to V_{SS}.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le 125°C$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage 2/	V_{OH}	I_{OUT} = -1 mA	1, 2, 3	All	2.4		V
Low level output voltage 2/	V_{OL}	I_{OUT} = 4 mA	1, 2, 3	02,03, 06,07,08		0.4	V
		I_{OUT} = 2.1 mA		04,05		0.4	V
Output leakage current	I_{OL}	OE = V_{IH}	1, 2, 3	All	-50	+50	µA
Input leakage current	I_{IL}		1, 2, 3	All	-10	+10	µA
Average V_{CC} current	I_{CC1}	T_C = 25°C and -55°C	1, 2, 3	01,02, 03,04, 05		120	mA
				06,07,08		180	mA
	I_{CC2}	T_C = +125°C	1, 2, 3	01,02, 03,04, 05		90	mA
				06,07,08		180	mA
Input capacitance 3/, 4/	C_I	Except DO thru D7	4	02,03		4	pF
				04,05		8	pF
				06,07,08		6	pF
Input capacitance 3/,4/	C_O	DO thru D7; OE = V_{IH}	4	All		10	pF
Functional tests 5/			8	All			
Read cycle time (See figure 4) 6/	t_{RC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	02,07	120		ns
				03,04, 05,08	200		ns
				06	90		ns
Address access time (See figure 3) 6/	t_{AA}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	02,07		120	ns
				03,04, 05,08		200	ns
				06		90	ns
Chip enable access time 6/	t_{CEA}	$\overline{OE}$ = V_{IL}	9, 10, 11	02		60	ns
				03,04,05		100	ns
				06		90	ns
				07		120	ns
				08		200	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/, 6/ $-55°C \le T_C \le 125°C$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip enable data off time 7/	t_{CEZ}	$\overline{OE} = V_{IL}$	9, 10, 11	02,03	5	35	ns
Output enable access time	t_{OEA}	$\overline{CE} = V_{IL}$	9, 10, 11	02		60	ns
				03,04,05		100	ns
				06		50	ns
				07		70	ns
				08		80	ns
Output enable data off time 7/	t_{OEZ}	$\overline{CE} = V_{IL}$	9, 10, 11	02,03	5	35	ns
Address data off time	t_{AZ}	$\overline{CE} = OE - V_{IL}$	9, 10, 11	01,02, 03,04,05	5		ns
Output in high - Z from $\overline{OE}$	t_{OHZ}	$\overline{CE} = V_{IL}$	9, 10, 11	06		35	ns
				07		45	ns
				08		50	ns
Write cycle time (See figure 5)	T_{WC}	$\overline{WE} = \overline{CE} = V_{IL}$	9, 10, 11	02,07	120		ns
				03,04, 05,08	200		ns
				06	90		ns
Address setup time	t_{AS}	$\overline{CE} = V_{IL}$	9, 10, 11	02,03	0		ns
				04,05,08	20		ns
				06,07	10		ns
Address hold time	t_{AH}	$\overline{CE} = V_{IL}$	9, 10, 11	02	40		ns
				03	65		ns
				04,05	0		ns
Data to write setup time	t_{DSW}	$\overline{WE} = CE = V_{IL}$	9, 10, 11	02	10		ns
				03	20		ns
				04,05	80		ns
				06	35		ns
				07	45		ns
				08	60		ns
Data from write hold time	t_{DHW}	$\overline{CE} = V_{IL}$	9, 10, 11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/, 6/ $-55°C \le T_C \le 125°C$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write pulse duration	t_{WD}	$\overline{CE} = V_{IL}$	9, 10, 11	02	45		ns
				03	60		ns
				04, 05	100		ns
				06	55		ns
				07	70		ns
				08	100		ns
Write enable data off time	t_{WEZ}	$\overline{CE} = V_{IL}$	9, 10, 11	02, 03	5	35	ns
				04, 05	60		ns
Write pulse lead time 7/	t_{WPL}	$\overline{CE} = V_{IL}$	9, 10, 11	02	65		ns
				03	130		ns
Output hold time from address change	t_{AH}		9, 10, 11	06,07,08	5		ns
Output in low-Z from $\overline{CE}$	t_{CLZ}		9, 10, 11	06,07,08	5		ns
Output in high-Z from $\overline{CE}$	t_{CHZ}		9, 10, 11	06		40	ns
				07		50	
				08		55	
Output in low-Z from $\overline{OE}$	t_{OLZ}		9, 10, 11	06,07,08	5		ns
Chip selection to power up time	t_{PU}		9, 10, 11	06,07,08	0		ns
Chip deselection to power down time	t_{PD}		9, 10, 11	06		45	ns
				07		55	
				08		60	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/, 6/ $-55°C \le T_C \le 125°C$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write recovery time	t_{WR}		9, 10, 11	06,07,08	5		ns
Output in low-Z from $\overline{WE}$	t_{WLZ}		9, 10, 11	06,07,08	5		ns
Output in high-Z from $\overline{WE}$	t_{WHZ}		9, 10, 11	06 07, 08		35 50	ns
Address valid to end of write	t_{AW}		9, 10, 11	06 07 08	80 105 120		ns

1/ All voltages referenced to V_{SS}.

2/ Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

3/ Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts and $V_{CC} = 5.0$ V

4/ For subgroup 4 see 4.4.1c.

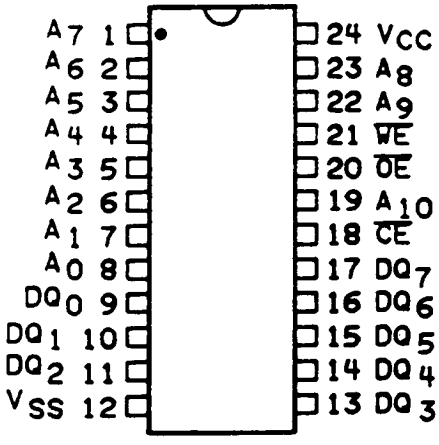
5/ For subgroup 8 see 4.4.1d.

6/ AC measurements assume transition time = 5 ns and input levels are from V_{SS} to 3.0 V.

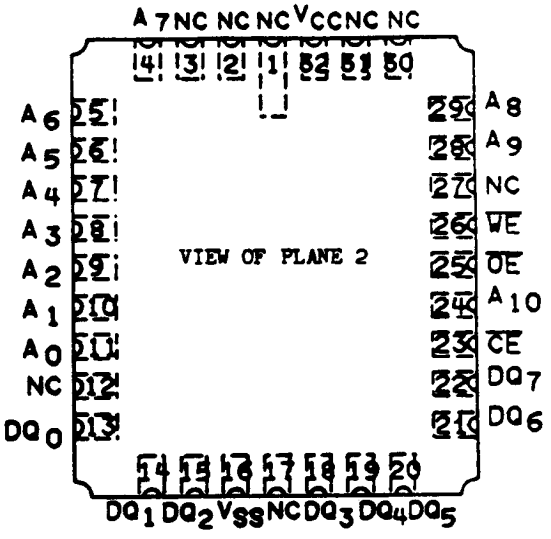
7/ These three tests not performed for device types 04, 05, 06, 07 and 08.

Device types 01, 02, 03, 04, 05, 06, 07, and 08.

CASE J



CASE Z



OPTION A WITH ACTIVE TERMINALS ON PLANE 1

PIN NAMES

A_0 - A_{10}	Address Inputs
$\overline{CE}$	Chip Enable
V_{SS}	Ground
DQ_0 - DQ_7	Data In/Data Out
V_{CC}	Power (+5 V)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

FIGURE 1. Terminal connections.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ
V_{IH}	X	X	DESELECT	HIGH Z
V_{IL}	X	V_{IL}	WRITE	D_{IN}
V_{IL}	V_{IL}	V_{IH}	READ	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z

X = DON'T CARE

FIGURE 2. Truth table.

Device 01-05

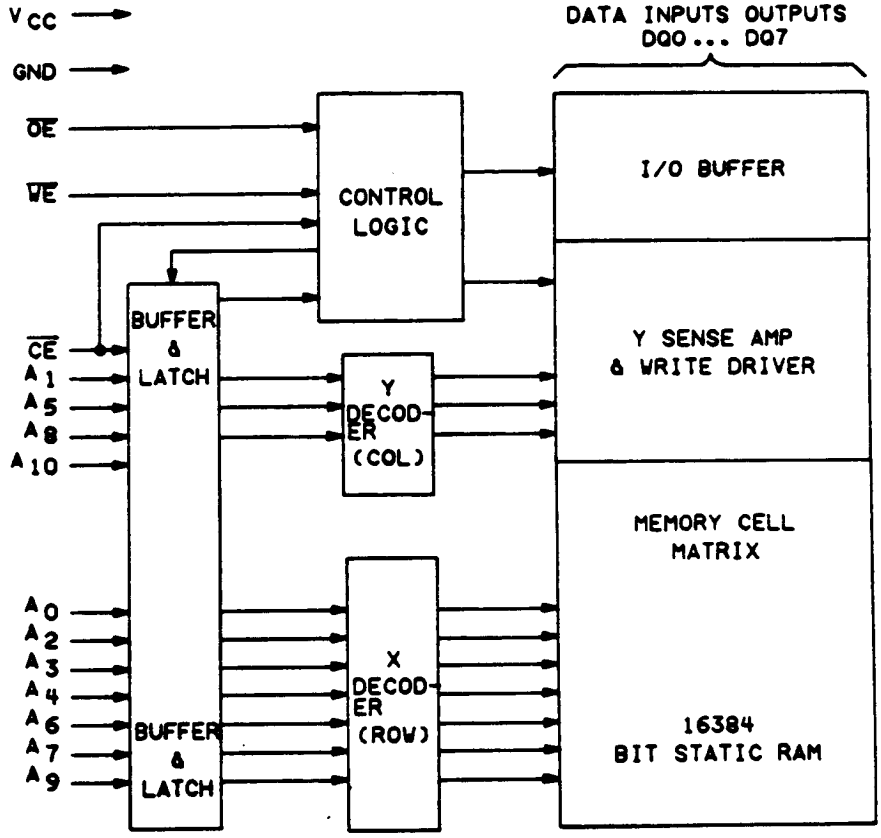


FIGURE 3. Block diagram.

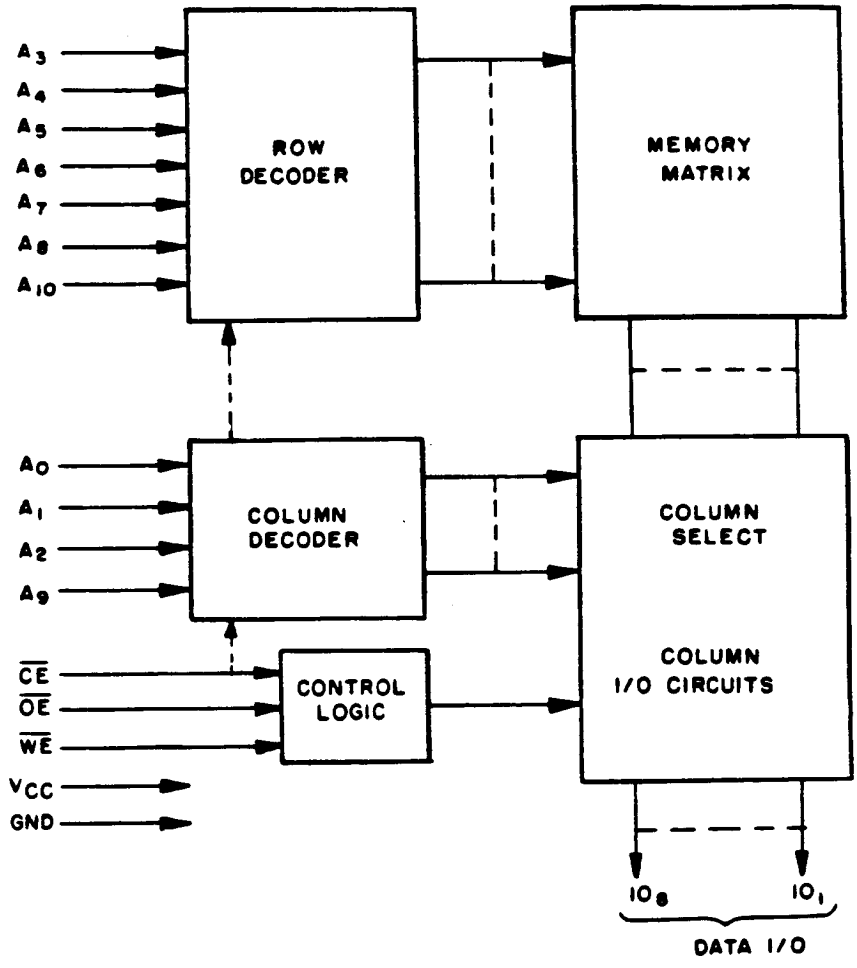
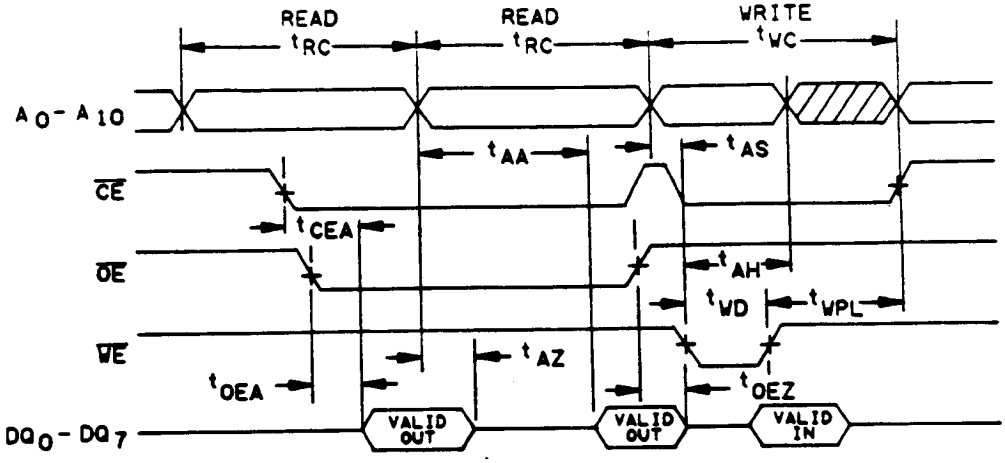


FIGURE 3. Block diagram - Continued.

Device 01-05



Device 06-08

READ CYCLE 1

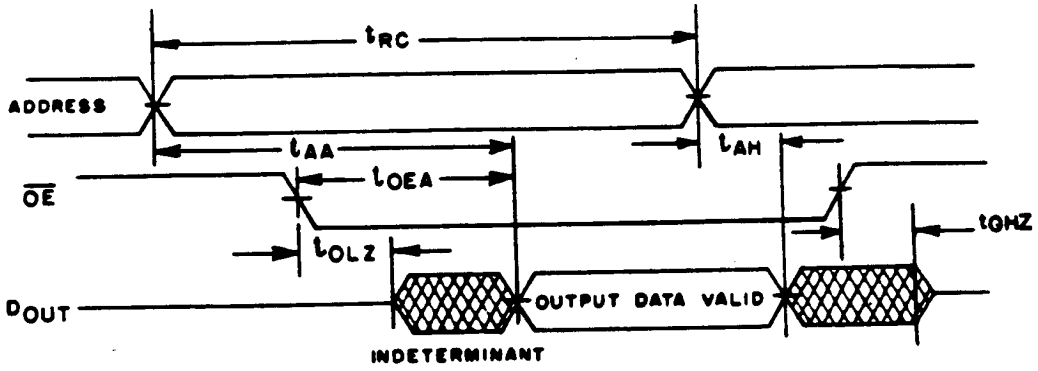


FIGURE 4. Read cycle timing diagram.

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READ CYCLE 2

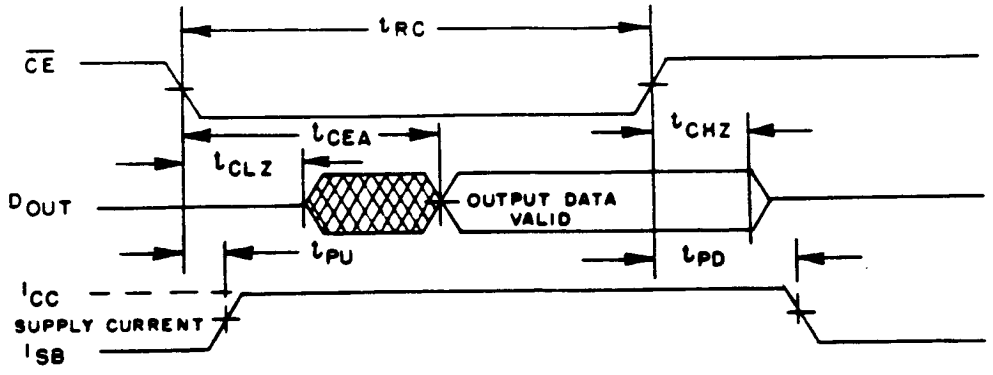


FIGURE 4. Read cycle timing diagram - Continued.

Device 01-05

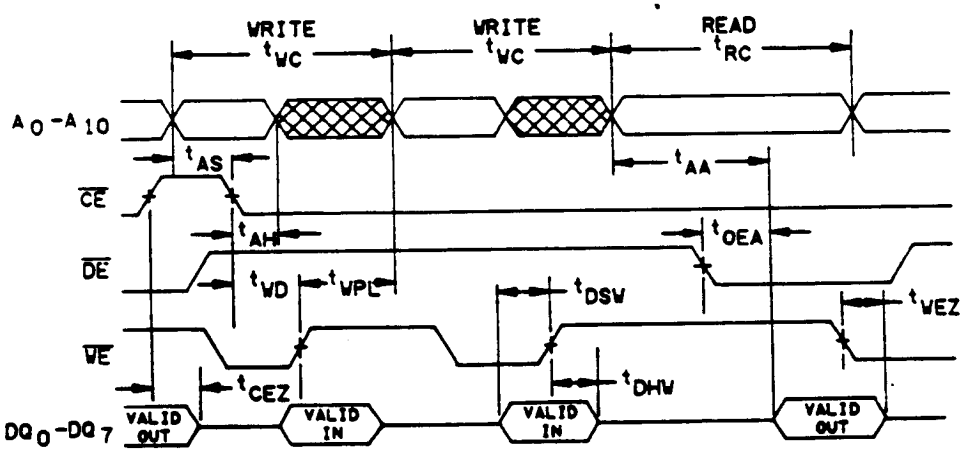
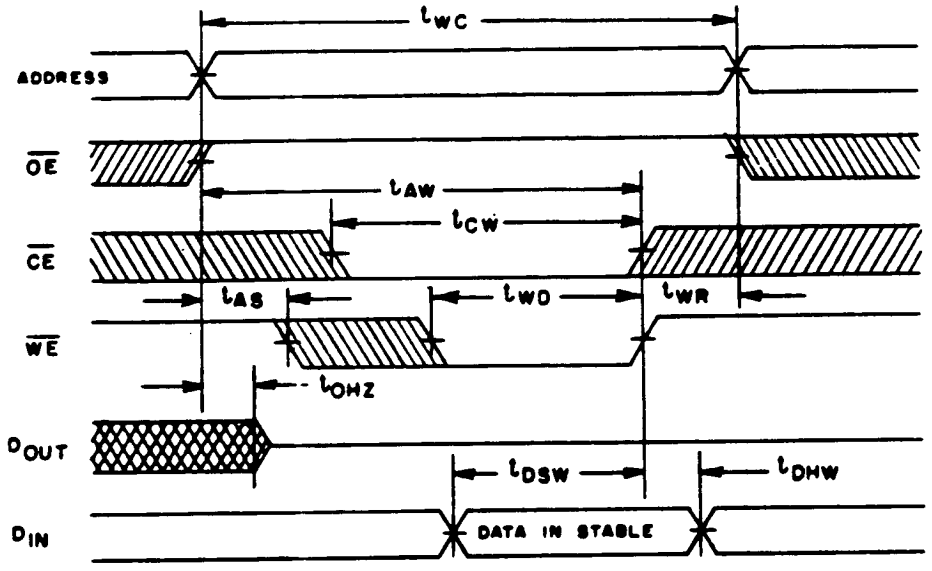


FIGURE 5. Write cycle timing diagram.

WRITE CYCLE 1



WRITE CYCLE 2

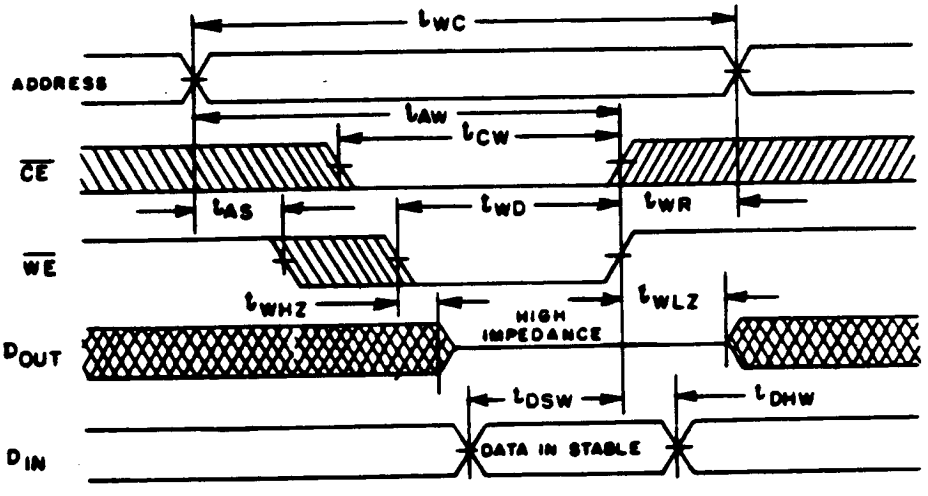


FIGURE 5. Write cycle timing diagram - Continued.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.5 Marking. Marking shall be in accordance with MIL-M-38510 except the part number shall be in accordance with 1.2 herein. The Vendor Similar Part Number may also be marked in accordance with 6.9 herein. Both part numbers, when used, shall be printed on the same surface. The "M38510/XXX" part number and the "JAN" or "J" mark shall not be used. Lead finish letter "X" is used only as specified in MIL-M-38510 and shall not be marked on the microcircuit or its packaging. The country of origin shall be marked on the microcircuit.

3.6 Quality assurance requirements. Microcircuits furnished under this drawing shall have been subjected to, and passed all the requirements, tests, and inspections detailed herein including screening and quality conformance inspections.

3.6.1 Screening. Screening shall be in accordance with method 5004, class B, of MIL-STD-883 and 4.2 herein.

3.6.2 Qualification. Qualification inspection for the device types specified herein shall not be required.

3.6.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and 4.4 herein.

3.6.4 Burn-in test circuit documentation. The burn-in test circuit documentation shall be made available to the acquiring activity on request.

3.7 Manufacturer eligibility. To be eligible to supply microcircuits to this drawing, a manufacturer shall have manufacturer certification in accordance with MIL-M-38510 for at least one line and have part I listing on Qualified Products List QPL-38510 for at least one device type (not necessarily the one for which the acquisition of this drawing is to apply).

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply (see 6.8 and 6.9).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection for the device types specified herein shall not be required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Groups A and B inspections shall be performed on each inspection lot or as specified in method 5005, of MIL-STD-883. Groups C and D shall be performed on a periodic basis in accordance with MIL-M-38510. Generic test data (see 6.5) may be used to satisfy the requirements for groups C and D inspections. Manufacturers shall keep lot records for 5 years (minimum), monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records, including an attributes summary of all screening and quality conformance inspections conducted on each lot shall be available for review by customers at all times.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 8, 9, 10, 11**
Group A test requirements (method 5005)	1, 2, 3, 4, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 9
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1 (see 4.2c).
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883, class B, and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 7 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{in} measurement) shall be measured only after the initial test and after process or design changes which may affect input capacitance. Generic test data (6.5) may be used to satisfy the subgroup 4 requirement.

d. Subgroup 8 tests sufficient to verify the truth table.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table IIb of method 5005 of MIL-STD-883, class B.

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV of method 5005 of MIL-STD-883, class B, and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. Only the note "Reevaluation of lot quality" of the notes specified in MIL-M-38510 shall apply to this drawing.

6.2 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of unnecessary duplicate specifications, drawings, and stock catalog listings. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, this drawing will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity, if applicable.

e. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct shipment to the Government.

6.4 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.5 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.1c. and 4.4.3. Group C generic test data shall be on date codes no more than 1 year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D generic data shall be on date codes no more than 1 year old and on the same package type (terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 5 years from the date of shipment.

6.6 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment, tools, and operator.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

6.8 Submission of certificate of compliance. The certificate of compliance submitted to DESC-ECS, prior to listing as an approved source of supply in 6.9, shall state that the manufacturer's product meets the provisions for MIL-STD 883 compliant devices and the requirements herein.

6.9 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.8) has been submitted to DESC-ECS.

DESC drawing part number	Vendor FSCM number	Vendor similar part number 1/
8103901JX	---	2/
8103901ZX	---	2/
8103902JX	---	2/
8103902ZX	---	2/
8103903JX	---	2/
8103903ZX	---	2/
8103904JX	---	2/
8103904ZX	---	2/
8103905JX	---	2/
8103905ZX	---	2/
8103906JX	34335	AM9128-90/BJA
8103907JX	34335	AM9128-12/BJA
8103908JX	34335	AM9128-20/BJA

1/ CAUTION: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Not available from an approved source.

Vendor FSCM number	Vendor name and address
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086